

Appl. No. 10/707,396
Amdt. dated April 22, 2005
Reply to Office action of January 26, 2005

Listing of Claims:

Claim 1 (Previously presented): A vertical dynamic random access memory (DRAM) comprising:

- a substrate comprising at least a deep trench having an upper trench portion and a lower trench portion;
- 5 a trench capacitor located in the lower trench portion;
- a source-isolation oxide layer located on the trench capacitor;
- a shallow trench isolation (STI) positioned around the deep trench; and
- a vertical transistor located on the source-isolation oxide layer, the
- 10 vertical transistor comprising:
- an annular source set in the substrate next to the source-isolation oxide layer, the annular source being electrically connected to the trench capacitor;
- a gate conductive layer filling the upper trench portion and
- 15 electrically connected to a first contact plug;
- a cylindrical gate dielectric layer located on a surface of a sidewall of the upper trench portion and circularly encompassing the gate conductive layer; and
- an annular drain circularly encompassing the deep trench near a
- 20 surface of the substrate, the annular drain being positioned next to the STI and electrically connected to a second contact plug, and being isolated from the annular drains of adjacent vertical transistors by the STI.

25 **Claim 2 (original): The vertical DRAM of claim 1, wherein the trench capacitor comprises:**

- a storage node filling the lower trench portion and electrically connected to the annular source;
- a capacitor dielectric layer encompassing the storage node; and

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a buried plate located in the substrate in a side of the capacitor dielectric layer.

Claim 3 (original): The vertical DRAM of claim 2, wherein the buried plate 5 surrounds a sidewall of the lower trench portion, and the capacitor dielectric layer is located on a surface of the sidewall of the lower trench portion so as to isolate the storage node and the buried plate.

Claim 4 (original): The vertical DRAM of claim 2, wherein the trench 10 capacitor further comprises a buried strap for electrically connecting the annular source and the storage node.

Claim 5 (Previously presented): The vertical DRAM of claim 4, wherein the buried strap is an annular conductive strap located on the inner surface 15 of the sidewall of the lower trench portion above the capacitor dielectric layer.

Claim 6 (original): The vertical DRAM of claim 1, wherein the vertical DRAM further comprises a conductive layer located on the gate conductive 20 layer for electrically connecting the gate conductive layer and the first contact plug.

Claim 7 (original): The vertical DRAM of claim 1, wherein the annular source is an ion diffusion area.

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Claim 8 (original): The vertical DRAM of claim 1, wherein the annular drain overlaps a heavily doped ion implantation area.

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Claim 9 (original): The vertical DRAM of claim 1, wherein the vertical DRAM further comprises a passivation layer covering the surface of the substrate and the transistor.

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Claim 10 (original): The vertical DRAM of claim 1, wherein the first and the second contact plug are electrically connected to a word line and a bit line respectively.

10 **Claim 11 (Previously presented):** The vertical DRAM of claim 1, wherein the shallow trench isolation surrounds the annular source and the annular drain without overlapping the deep trench.

15 **Claim 12 (Previously presented):** The vertical DRAM of claim 1, wherein the vertical DRAM further comprises an annular spacer surrounding the upper trench portion.

20 **Claim 13 (Previously presented):** The vertical DRAM of claim 12, wherein the second contact plug has an asymmetric structure, which is positioned on the spacer and the annular drain while contacts the spacer and the annular drain at the same time.